REMARKS

In the Office Action, the Examiner rejected noted the requirement for a separate listing of prior art in order for the art to be considered, approved the drawings, rejected claims 16 and 20 – 33 [sic, assumed to be 16 and 20 - 32] under the first paragraph of section 112, rejected claims 16-26 and 29 – 30 as anticipated by Hsu, and rejected claims 27 and 28 as obvious over Hsu in view of Ludikhuize.

Information Disclosure Statement

An Information Disclosure Statement was filed in the present application on May 2, 2000, accompanied by copies of prior art documents and a Form 1449 listing the prior art. Receipt of the Information Disclosure Statement by the Patent Office was acknowledged by returned post card receipt, and by the Notification of Acceptance of Application Under 35 USC 271 and 37 CFR 1.494 or 1.495. A review of the Examiner's Actions finds that the 1449 form and the art cited therein has not been acknowledged by the Examiner.

Accordingly, the Examiner's attention is directed to the prior art submitted with the Information Disclosure Statement of May 2, 2000. Favorable consideration of the present application in view of the submitted art is hereby requested.

35 U.S.C. §112, 1st ¶

Applicants respectfully disagree with the Examiner's characterization of the specification as failing to disclose that the inventors had possession of the claimed invention.

As is clear from a review of the present application, the present invention, in one embodiment, is directed to an edge structure of a high voltage semiconductor chip. The high

voltage chip includes a number of high voltage elements. The high voltage elements located away from the edge of the chip operate in the desired manner, but the high voltage elements near the edge of the chip suffer from the effects of a voltage drop-off at the chip edge, leading to undesirable performance of these elements near the edge. In the present invention, an edge structure is provided at or near the chip edge to avoid or reduce the voltage drop off and ensure the desired performance of the high voltage elements near the edge.

The edge structure of the present invention forms a ring or boundary around the high voltage elements and a barrier between the high voltage elements and the edge of the chip. The edge structure is such that the voltage level is maintained across the chip all the way to the elements near the edge.

Quoting from the English translation of the specification as filed, "In semiconductor elements, particularly in high voltage resistant power semiconductor components, voltage breakthroughs preferably arise in their edge region outside the doping zones, since the electrical field intensity is especially great there due to the curvature of the doping zones which is conditioned by the edge. To avoid such voltage breakthroughs, doping zones are arranged in rings about the semiconductor components. These annular doping zones reduce local field intensity peaks in the edge region of the semiconductor component." (page 1, lines 12 – 18)

Further quoting from the specification, "US 3,405,329 teaches edge structures of semiconductor components with what are known as magnetoresistive rings. These magnetoresistive rings are constructed so as to achieve a largely uniform voltage distribution along the surface of the semiconductor body of a semiconductor component. In this way, field

intensity peaks which favor the occurrence of a breakthrough are avoided." (page 1, line 25, to page 2, line 2)

In describing the invention, the specification provides, "The semiconductor component comprises a cell field ZF consisting of a plurality of individual components, which are connected in parallel and are arranged in individual cells Z1...Z3, ... The cell field ZF is terminated by an edge structure that is provided in the edge region RB of the semiconductor component. The edge region RB refers to the region of the semiconductor component located outside its active cells Z1...Z3 of the cell field ZF." (page 6, lines 4 to 10)

Thus, the application as filed discloses the features noted by the Examiner and the claims meet the requirements of the first paragraph of section 112.

35 U.S.C. §102(b)

The Hsu reference shows in Figure 1 a lateral MOSFET having an n-doped source zone 14, a p-doped body zone, an n-doped drift zone 12 and an n-doped drain zone 16. Above the body zone 10 and extending from the source zone 14 to the drift zone 12 is a gate electrode 26 that is isolated against the semiconductor zones. The drift zone 12 has several p-doped zones 18 below the surface of the semiconductor body.

The Hsu reference does not disclose an edge structure of a semiconductor device. Applicants note the Examiner's statement that the heavily doped region 16 of Figure 1 of Hsu is a space charge zone stopper. However, the specification at column 1, lines 46 – 52, describes the N+ regions of the semiconductor device as the source and drain regions. Thus, these regions are not space charge zone stoppers.

In Hsu is disclosed a lateral MOSFET. According to the present invention, by contrast, an edge structure or edge termination of a semiconductor device is provided, wherein the edge termination surrounds high voltage semiconductor devices, for example, vertical MOSFETs.

The features of the invention which distinguish over the Hsu reference provides for a cell field including a plurality of individual components which are connected in parallel and are arranged in individual cells. The high voltage edge structure surrounds the cell field.

At least one floating guard ring and one inter-ring zone are arranged adjacent to each other.

The claims have been amended to claim features which further distinguish over the Hsu reference. Favorable reconsideration of the claims is hereby requested.

Although claims 31 and 32 are not rejected under section 102, they are discussed in the text following the rejection and so are treated here as rejected. If this is not the case, the Examiner is respectfully requested to so indicate.

35 U.S.C. §103(a)

Even when combined with the teachings of Ludikhuize, the Hsu reference fails to suggest the edge structure of the present invention.

The present invention as claimed is thus not shown or suggested in the prior art, and therefore is a non-obvious improvement thereover.

Conclusion

Each issue raised in the action has been addressed. Early favorable reconsideration and allowance is hereby requested.

Respectfully submitted,

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